**Introduction**

During the Spring 2023 school semester, I took my first Computer Architecture class, CprE 381, at Iowa State University. In this class, we learned how to convert basic programs into assembly, design and analyze a MIPS processor, and compare different cache designs. In the lab portion of the class, we focused on implementing three different MIPS processors using VHDL and ModelSim, including a single cycle, 5 stage software pipeline, and 5 stage hardware pipeline processor. We started with the single cycle processor, and designed modules to increment the program counter, decode instructions, a register file, a sign extender, and an ALU. For the 5 stage processors, we broke apart each of these components into five separate stages, so that we could reduce the critical path latency and improve the maximum clock rate of our design. Near the end of the project, me and my partner had about a month of time left. Due to this, we decided to work on an extra credit project through the form of an FPGA wrapper with the Altera DE2 FPGA Development board. For more information on each of these designs, please look at the other tabs for this project.

The goal of this project was to learn more about implementing specific components of a processor, and analyzing the performance tradeoffs between each of our three processors. For the software pipeline, we inserted NOP instructions to remove the risk of data and control dependencies within our pipeline. This led to an increased number of instructions, which made our overall execution time larger. As we implemented stalling in the pipeline registers of our hardware pipeline, we were able to reduce the number of instructions used, with the tradeoff of our CPI increasing from a near average of 1. After adding forwarding we were able to reduce the average CPI of our hardware pipeline while retaining a faster maximum clock frequency compared to our single cycle design. By analyzing these choices, we were able to make educated design decisions on how to improve our HW pipeline design, and yield an improved performance compared to our first two processor designs.

Another goal of the project was to take ownership in our required work by taking it a step further with an extra credit project. As mentioned before, we had extra time near the end of the semester, so me and my partner Thomas worked on designing an FPGA wrapper for the Altera DE2 FPGA development board. With this, we were able to combine Verilog code from our previous digital design class, that I also was a teaching assistant for, and a mix of FPGA modules, from the previous library I designed, to make a robust wrapper. It was very satisfying to combine designs for clock dividers, button debouncers, and seven segment display interfaces that had already been extensively tested, and apply them to an interesting and challenging MIPS processor design. This was also a fantastic goal and achievement since we were finally able to see our processor run on real hardware, and not just the required simulations for the course and lab. For more information, please reference the FPGA tab on this page.

**Single Cycle Processor**

**5 Stage Processor**

**FPGA Wrapper**